Freescale Semiconductor

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# PCIe Certification Guide for i.MX 6Dual/6Quad and i.MX 6Solo/6DualLite

This document provides a description of procedures, tools, and criteria for the PCI Express (PCIe) Gen2 electrical compliance test for the following i.MX 6 series chips: i.MX 6Quad, i.MX 6Dual, i.MX 6DualLite, and i.MX 6Solo.

Contents



## 1 Test equipment

### 1.1 Test board

The test is performed on the following boards:

- MCIMX6QAI
- MCIMX6SAI

### 1.2 Measurement equipment

The following equipment is used to measure signal quality:

- Oscilloscope: Tektronix MSO72004C
- Probes: Tektronix P7313SMA (4)
- Cables: Rosenberger P/N 71M-19K1-32S1-01000A
- Test Fixture: CLB2 X1
- Power Supply: SunPower P40A-1P2J

## 1.3 Test environment

- Operation System: Linux L3.0.35_12.11.01_GA
- Additional software changes for PCIe compliance test based on L2.6.35_1.0.0 are required. To access software changes and updated test images, visit https://community.freescale.com/docs/DOC-94923.

## 1.4 Analysis software

- SigTest Version 3.1.60

## 1.5 Additional information

- Test items: only contains the electrical test
- Test method and equipment operation:
  - See *PCI Express® Architecture PHY Test Specification*, rev. 2.0. (PCI-SIG: 2008, pcisig.com .
  - See document #CLB_USAGE_DOC_Rev_1_4_DSA72000b, *PCI Express 2.0 CEM System Signal Quality and Reference Clock Jitter Test Methodology using Tektronix MSO/DPO/DSA72004 (20GHz), MSO/DPO/DSA71604 (16GHz) and MSO/DPO/DSA71254 (12.5GHz) Real Time Oscilloscopes*, rev. 1.4 (PCI-SIG, 2011; register at pcisig.com to download this document).
- 100 MHz reference clock: internal PLL clock[1]

# 2 Software configuration and procedures

## 2.1 TX test configuration and procedures

The following is an overview of the test steps:

1. Integrate the patch for the PCIe test to the mainline, recompile the kernel image[2], and replace the old image of the board under the test.

   Make sure the following configuration has been set when recompiling the kernel image.

   ```
   # MX6 Options:
   CONFIG_IMX_PCIE=y
   ```

1. The default clock source is the internal PLL clock. By default, the Linux BSP does not support the external 100 Mhz oscillator. Contact your local Freescale representative for support to use the external oscillator.
2. This patch only removes the clks/power release codes. For information on how to compile the kernel image, see either the *i.MX 6Dual/6Quad SABRE-SD Linux User's Guide* (IMX6DQLXUGSSD) (for i.MX 6Quad or i.MX 6Dual) or the *i.MX 6Solo/6DualLite SABRE-SDP Linux User's Guide* (IMX6DLLXUGSSD) (for i.MX 6DualLite and i.MX 6Solo) accompanying the Freescale Linux board support package (BSP).

2. Correctly set up the test environment:
   - Connect the compliance load board (CLB x1/x16) revision 2.0 into the DUT slot. Then, change the switch and jumpers to select x1 mode.[1]
   - Connect the lane under the test to the oscilloscope using a differential probe and matching coaxial cable[1]. The cable calibration should be done before the test.
   - Connect the clock signal to the oscilloscope. The clock must have the SSC enabled or disabled to be consistent with the settings for the system during normal operation.
   - Start up the system.
3. After i.MX 6 enters the polling.compliance stage[2], press the toggle button on CLB to select the output mode[3]. Ensure the data waveform is compliant with the pattern 5.0 GT/s for Gen2, and 2.5 GT/s for Gen1.
4. Follow operation instructions for the oscilloscope and ensure it is set to the right mode.
5. Capture and save at least 1 million * 200 ps of data while simultaneously clocking at the sample rate of 50 GS/s for Gen2, or 250,000 UI * 400 ps of data at the sample rate of 25 GS/s for Gen1.
6. Run free software SigTest to analyze the PCIE TX signal.
7. The parameters of PCIe_PHY can be adjusted by changing the IOMUXC_GPR8 register settings to get the test passed.
   a) [Code] The register default is configured as:

```
imx_pcie_clrset(IOMUXC_GPR8_TX_DEEMPH_GEN1, 0 << 0, IOMUXC_GPR8);
imx_pcie_clrset(IOMUXC_GPR8_TX_DEEMPH_GEN2_3P5DB, 0 << 6, IOMUXC_GPR8);
imx_pcie_clrset(IOMUXC_GPR8_TX_DEEMPH_GEN2_6DB, 20 << 12, IOMUXC_GPR8);
imx_pcie_clrset(IOMUXC_GPR8_TX_SWING_FULL, 127 << 18, IOMUXC_GPR8);
imx_pcie_clrset(IOMUXC_GPR8_TX_SWING_LOW, 127 << 25, IOMUXC_GPR8);
```

   b) [Command line entry after Linux boot] For register address, 20E_0000h base + 20h offset = 20E_0020h, write the command：

```
/unit_tests/memtool -32 0x020e0020= FFFD4000
```

8. Detailed information of the related register, IOMUXC_GPR8, is provided in the following table:

1. See the connection and configuration information in document #CLB_USAGE_DOC_Rev_1_4_DSA72000b (PCI-SIG, 2011, pp. 11–14).
2. After a far-end termination is determined to be present, the Link Training and Status State Machine (LTSSM) enters the polling.compliance state and begins transmitting the compliance pattern on all lanes. Users do not need to enter any command to force the system into the polling.compliance state after boot.
3. See the operation information in #CLB_USAGE_DOC_Rev_1_4_DSA72000b (PCI-SIG, 2011, p. 22).

**Table 2-1. IOMUXC GPR8 filed descriptions**

| Field | Description |
|---|---|
| 31–25<br>PCS_TX_SWING_LOW | PCIe_PHY–This static value sets the launch amplitude of the transmitter when pipe0_tx_swing is set to 1'b0 (default state).<br>7'hxx–TX launch amplitude swing_low value. |
| 24–18<br>PCS_TX_SWING_FULL | PCIe_PHY–This static value sets the TX driver to SWING_FULL value.<br>7'hxx–Gen2 TX SWING FULL value. |
| 17–12<br>PCS_TX_DEEMPH_GEN2_6DB | PCIe_PHY–This static value sets the TX driver de-emphasis value in the case where pipe0_tx_deemph is set to 1'b0 and the PHY is running at the Gen2 (6db) rate.<br>6'hxx–Gen2 (6db) de-emphasis value. |
| 11–6<br>PCS_TX_DEEMPH_GEN2_3P5DB | PCIe_PHY–This static value sets the TX driver de-emphasis value in the case where pipe0_tx_deemph is set to 1'b1 (the default setting) and the PHY is running at the Gen2 (3p5db) rate.<br>6'hxx–Gen2 de-emphasis value. |
| 5–0<br>PCS_TX_DEEMPH_GEN1 | PCIe_PHY–This static value sets the TX drvier de-emphasis value in the case where pipe0_tx_deemph is set to 1'b1 (the default setting) and the PHY is running at the Gen1 rate.<br>6'hxx–Gen1 de-emphasis value. |

# 3 Test results

## 3.1 TX test data summary

The i.MX 6 silicon passes all TX electrical tests. The following measurements show performance criteria.

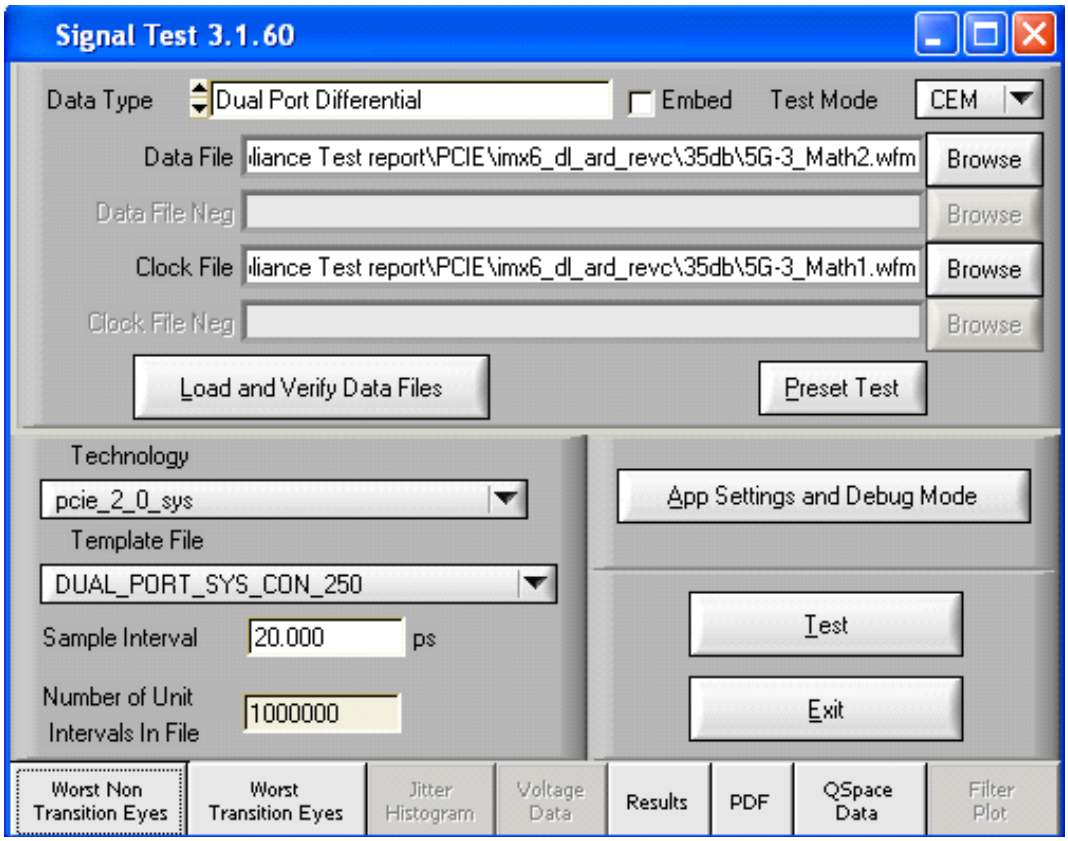


**Figure 1. SigTest test main window**

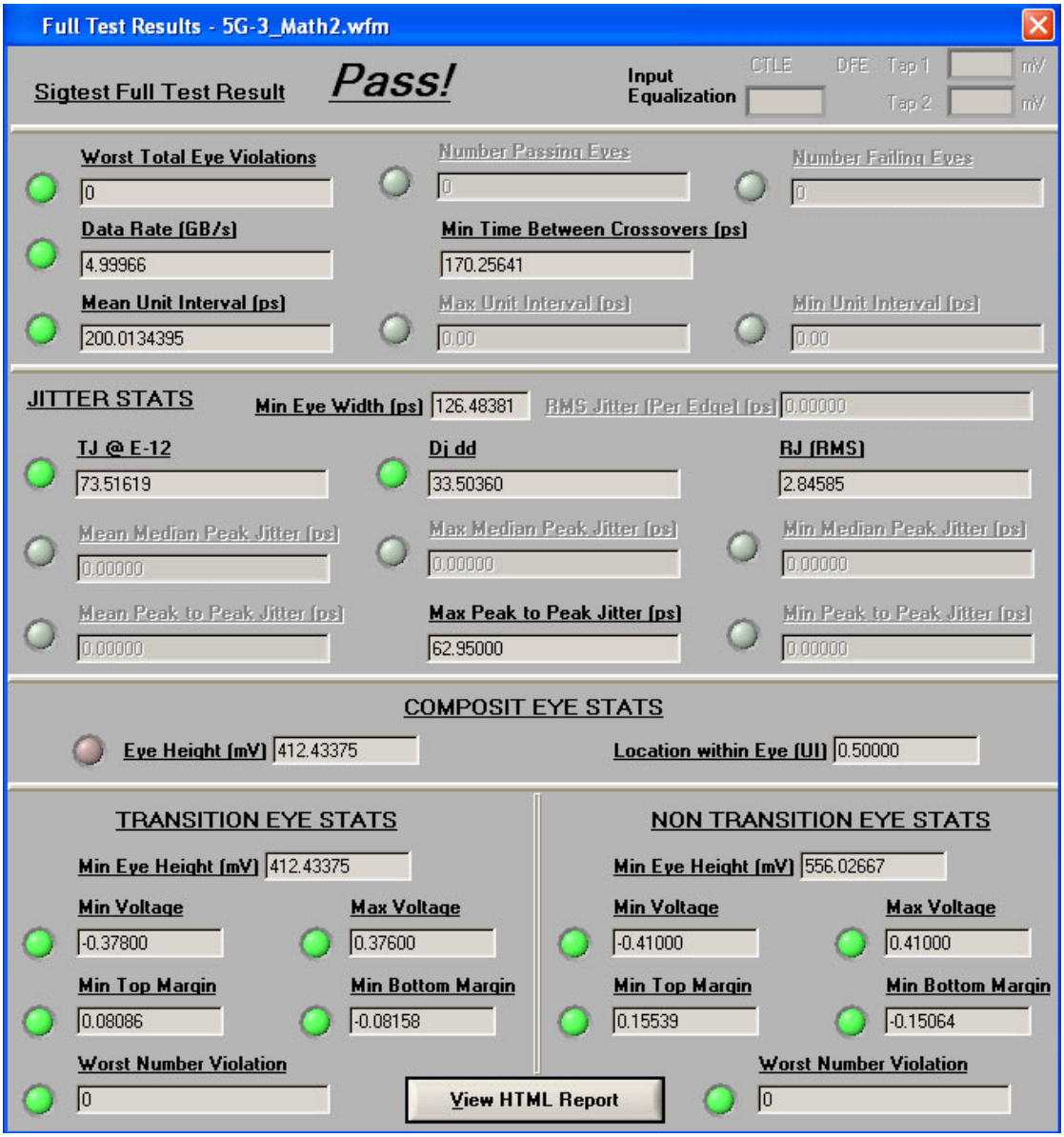


**Figure 2. GEN2 -3.5dB TX SigTest test result**

The generated HTML report is as follows:

Overall SigTest result: pass

- Mean unit interval (ps): 200.01344
- Min time between crossovers (ps): 170.25641
- Data rate (Gb/s): 4.999664
- Max peak to peak jitter: 62.950002 ps
- Total jitter at BER of 10E-12: 73.516193 ps
- Total jitter at BER of 10E-12 passes SigTest limits

- Minimum eye width: 126.483807 ps
- Deterministic jitter delta-delta: 33.503596 ps
- Deterministic jitter delta-delta passes SigTest limits
- Random jitter (RMS): 2.845846 ps
- Random jitter (RMS) passes SigTest limits
- Minimum transition eye voltage: -0.378 volts
- Minimum transition eye voltage passes SigTest limits
- Maximum transition eye voltage: 0.376 volts
- Maximum transition eye voltage passes SigTest limits
- Minimum nontransition eye voltage: -0.41 volts
- Minimum nontransition eye voltage passes SigTest limits
- Maximum nontransition eye voltage: 0.41 volts
- Maximum nontransition eye voltage passes SigTest limits
- Composit eye height: 0.412434
- Composit eye location: 0.5
- Minimum transition eye voltage margin above eye: 0.080856 volts
- Minimum transition eye voltage margin above eye passes SigTest limits
- Minimum transition eye voltage margin below eye: -0.081577 volts
- Minimum transition eye voltage margin below eye passes SigTest Limits
- Minimum transition eye height: 0.412434 volts
- Minimum nontransition eye voltage margin above eye: 0.155389 volts
- Minimum nontransition eye voltage margin above eye passes SigTest limits
- Minimum nontransition eye voltage margin below eye: -0.150638 volts
- Minimum nontransition eye voltage margin below eye passes SigTest limits
- Minimum nontransition eye height: 0.556027 volts

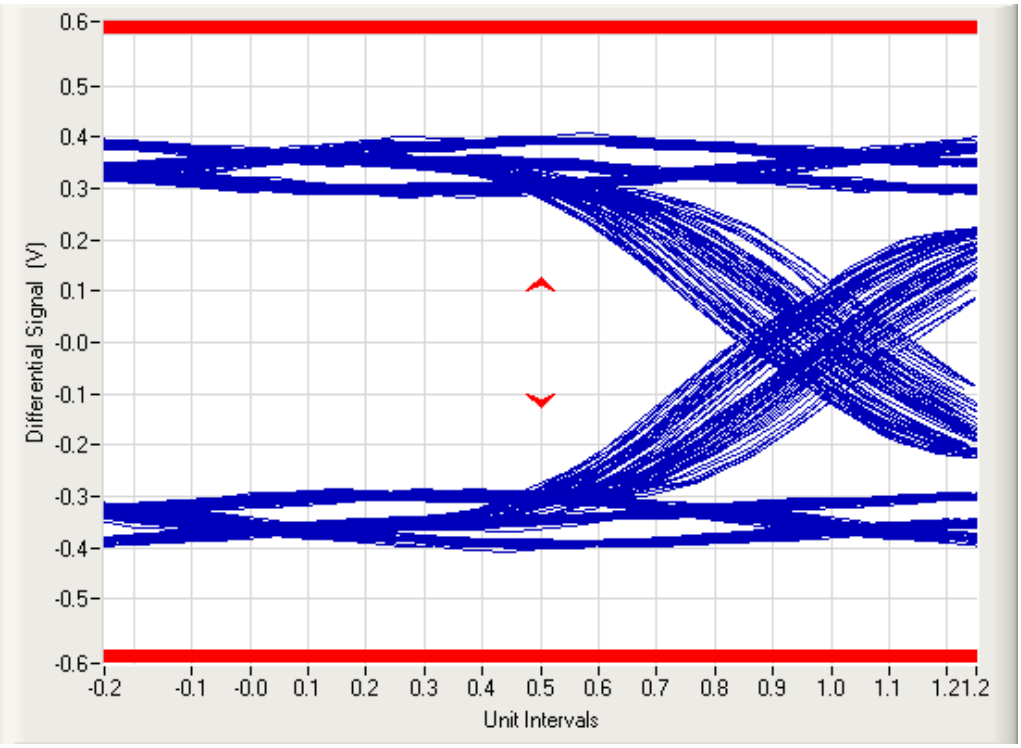


**Figure 3. Gen2 TX -3.5dB Worst nontransition signal eye**

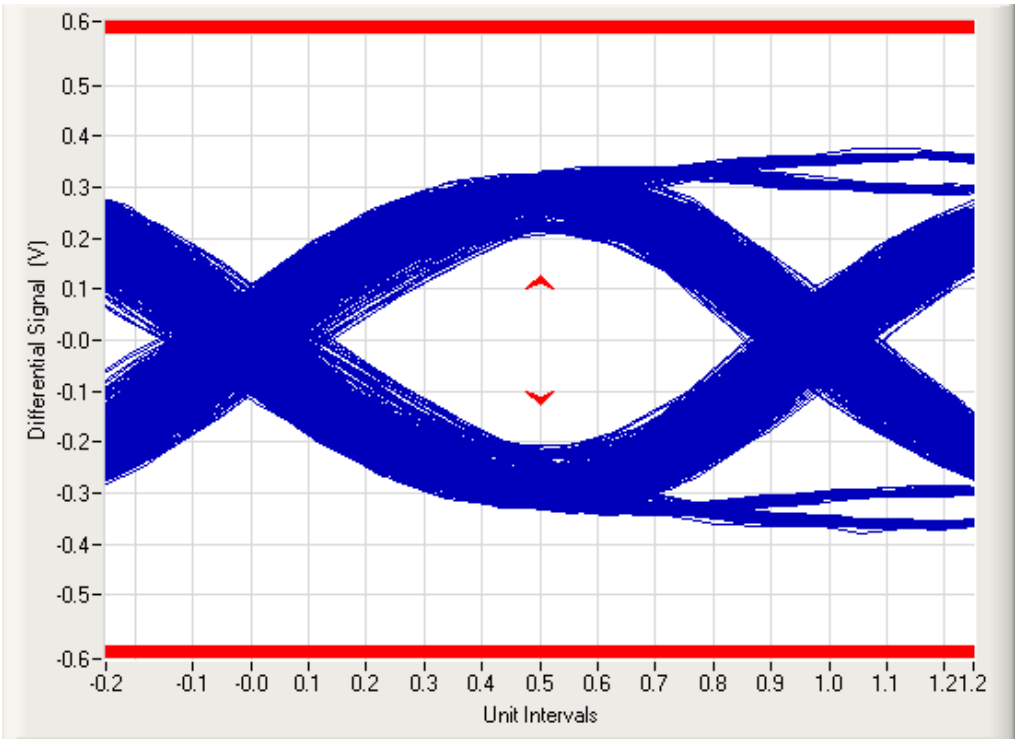


**Figure 4. Gen2 -3.5dB Worst transition signal eye**

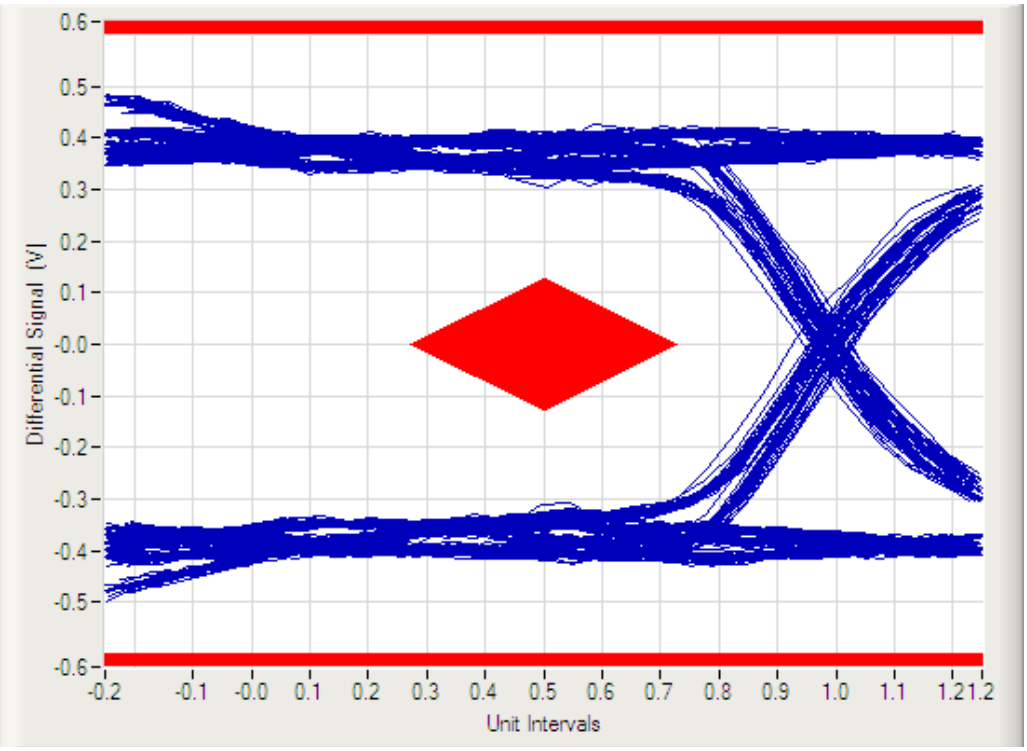


**Figure 5. Gen1 TX -3.5dB Worst nontransition signal eye**

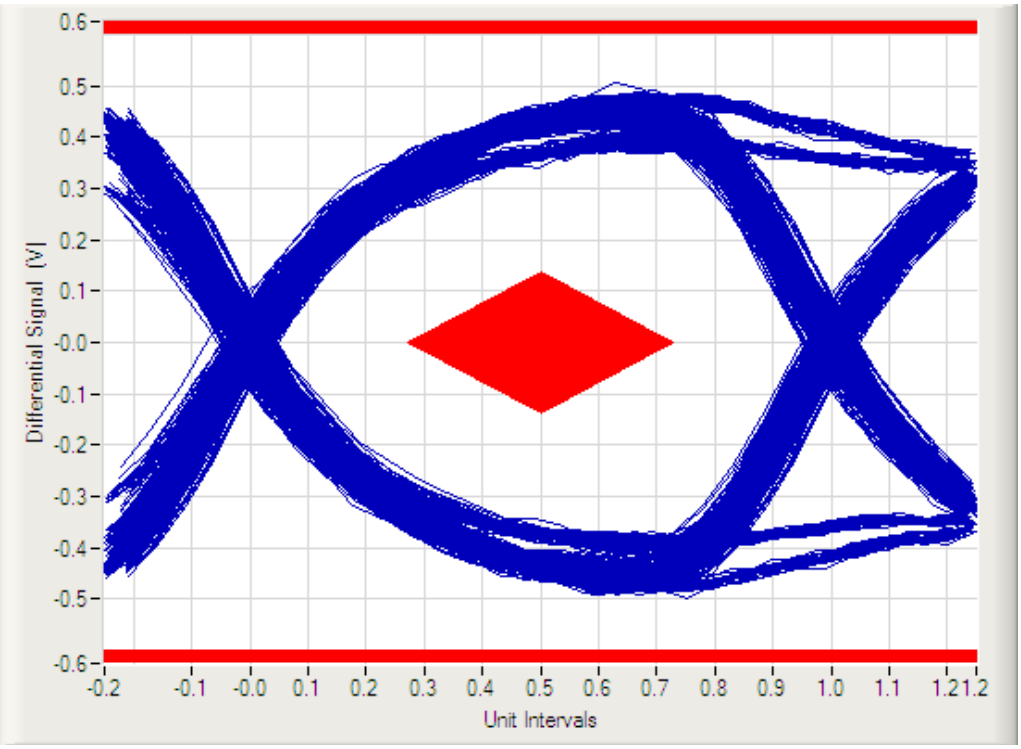


**Figure 6. Gen2 -3.5dB Worst transition signal eye**

# 4 Revision history

The following table provides a revision history for this application note.

**Table 4-1. Revision History**

| Rev. Number | Date | Substantive Change |
|---|---|---|
| 0 | 8/2013 | Initial release |


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