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i.MX 6Dual/6Quad and i.MX 6DualPlus/6QuadPlus Applications Processor Comparison

1 Introduction

This document describes the differences between the i.MX 6DualPlus/6QuadPlus and the i.MX 6Dual/6Quad from a customer perspective and will facilitate the mapping of high-level architectures to marketing requirements with sufficient detail to enable hardware and software planning.

More information about the i.MX 6Dual/6Quad can be found in the reference documents listed in Section 21, "References."

For i.MX 6DualPlus/6QuadPlus, this document will direct the reader to the appropriate sections of the i.MX 6DualPlus/6QuadPlus reference manual and datasheet, wherein detailed technical information on the differences can be found.

1.1 i.MX 6DualPlus/6QuadPlus overview

The i.MX 6DualPlus/6QuadPlus has been productized to meet higher graphics performance requirements. The goal of i.MX 6DualPlus/6QuadPlus is to significantly increase the

Contents

overall memory bandwidth of GPU to provide better visual performance and higher frame rate for customer use cases, including:

- Instrument cluster (OpenGL ES)
- Infotainment (HTML5, HMI)
- Enhanced multi-display support

The performance improvement will be achieved through the following changes:

- Modify bus architecture to improve DRAM utilization.
- Update GPU to new version for performance improvement.
- Add PRE (Prefetch and Resolve Engine) to support unresolved frame buffer for display.

In order to allow customers to migrate from i.MX 6Dual/6Quad seamlessly, we have the following compatibility requirements on i.MX 6DualPlus/6QuadPlus:

- Pin-to-pin compatible, no ball map changes
- No PINMUX changes
- No IP version changes other than the internal bus structures, GPU, PRE and PRG
- No memory map change for existing IP modules
- All features supported on i.MX 6Dual/6Quad are supported on i.MX 6DualPlus/6QuadPlus to the greatest extent possible
- Software compatibility is mantained to the greatest extent possible

In additional to the changes mentioned above, there have been errata fixes on i.MX 6DualPlus/6QuadPlus. The errata document for i.MX 6Dual/6Quad (IMX6DQCE) can be found on www.freescale.com. All **ERR00xxxx** references relate to this document and further details can be found there.

1.2 i.MX 6DualPlus/6QuadPlus feature diagram

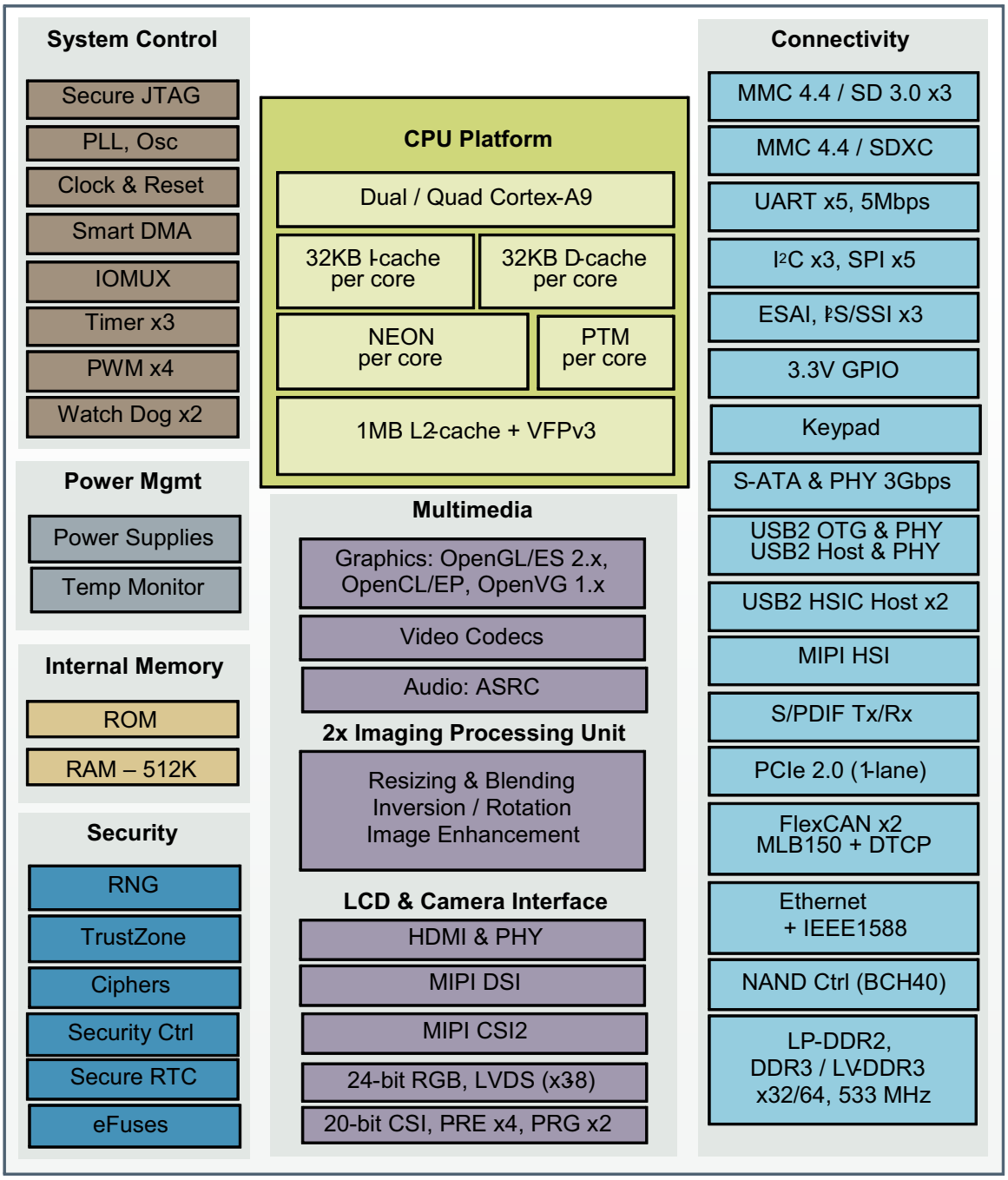

Figure 1. i.MX 6DualPlus/6QuadPlus Diagram

1.3 Feature change table

The following table is intended to summarize all the key improvements to the i.MX 6DualPlus/6QuadPlus with respect to i.MX 6Dual/6Quad.

Table 1. i.MX 6Dual/6Quad vs. i.MX 6DualPlus/6QuadPlus Changes

Category	Feature	Change	Comment/Justification
CPU	L2 Cache	Fixed an errata on L2 Cache controller so the double cache line fill function can be used	Improved memory access and performance efficiency
Bus	Fabric	Changed bus structure for key IP blocks	Optimized system performance
Memory	OCRAM	Added two OCRAM controllers with 128KB internal RAM attached to each controller	Used as pixel buffer for resolve and prefetch or as general purpose RAM when resolve and prefetch are not used
IRQ	Interrupt	Added interrupts for each of the PRE modules (PRE0-3)	—
Clock	CCM	Changed clock source and default frequency for some of the clock roots as well as clock gating improvements	IP frequency changes
Display	PRE	Added 4 PRE (Prefetch and Resolve Engine)	Used unresolved tile buffer from GPU for display to avoid resolve operation. Pixel prefetch to avoid IPU display FIFO underrun.
	PRG	Added 2 PRG (Prefetch and Resolve Gasket)	
	IPU	Added handshake signals with PRG.	
Graphics	GPU3D	Updated GC2000 with feature enhancements, new version is named as GC2000+	Graphics performance improvement and memory load optimization
	GPU2D	Updated GC320 with feature enhancements	
Others	—	Fixed several errata in i.MX 6Dual/6Quad	Further details in each section where relevant

2 ARM® Cortex®-A9 platform

Addressed errata ERR003740 (ARM errata number 752271)—to avoid causing data corruption in the double line fill feature—and ERR003742 (ARM errata number 732672) to enable double cache line fill operation in L2 cache controller. An abort on the second part of a double line fill can cause data corruption of the first part.

Before addressing these errata, the double cache line fill operation had to be disabled. In this case, the access from L2 cache to DRAM would be 32-bytes instead of 64-bytes. When 64-bit DDR3 is used, each burst access to the DRAM is 64-bytes. By addressing these errata, 100% DRAM efficiency improvement is achieved during L2 cache read accesses from 64-bit DDR3.

A newer version of the PL310 Cache Controller (PL310-r3p2) where the modified double line fill operation is used. In addition another PL310 errata ERR005199 (ARM errata number 769419)—No automatic Store Buffer drain, visibility of written data requires an explicit Cache Sync operation—has been addressed.

The rest of the Cortex-A9 platform design is reused from i.MX 6Dual/6Quad.

- Core Version MP004-BU-50000-r2p10-0rel0
- NEON™ Version AT397-BU-50001- r2p0-00rel0

3 System bus

The i.MX 6DualPlus/6QuadPlus bus architecture contains significant changes to achieve higher bandwidth and DRAM utilization. The key changes include:

- Optimized the internal bus configurations for GPU access to DRAM
- Increased bus width from 64 to 128-bit for GPU2D and GPU3D
- Added 4x AXI master ports for PRE modules
- Added 2x AXI slave ports for new OCRAM controllers used by PRE modules
- Updated bus controller connected to DRAM to include a scheduler for higher DRAM utilization. All other bus controllers will remain unchanged.
- Enabled scheduler bypass for dual-channel LPDDR2 use, allowing access to MMDC0/1 to remain symmetrical.

The AXI-ID for the bus masters have been updated on the i.MX 6DualPlus/6QuadPlus. Refer to the *i.MX 6DualPlus/6QuadPlus Applications Processor Reference Manual* (IMX6DQPRM) for details.

4 Memory map, interrupt and DMA

4.1 Memory map

The i.MX 6DualPlus/6QuadPlus contains four new PRE modules, two new PRG modules, and two new OCRAM. Memory map differences between i.MX 6Dual/6Quad and i.MX 6DualPlus/6QuadPlus are as follows.

Table 2. PRE and PRG Memory Map

Start	End	Size	i.MX 6Dual/6Quad	i.MX 6DualPlus/6QuadPlus
021C_F000	021C_FFFF	4KB	PERFMON3	Reserved
021C_E000	021C_EFFF	4KB		Reserved
021C_D000	021C_DFFF	4KB		PRG2
021C_C000	021C_CFFF	4KB		PRG1
021C_B000	021C_BFFF	4KB	PERFMON2	PRE3
021C_A000	021C_AFFF	4KB		PRE2
021C_9000	021C_9FFF	4KB		PRE1
021C_8000	021C_8FFF	4KB		PRE0
021C_7000	021C_7FFF	4KB	PERFMON1	Reserved
021C_6000	021C_6FFF	4KB		PERFMON3
021C_5000	021C_5FFF	4KB		PERFMON2
021C_4000	021C_4FFF	4KB		PERFMON1

Table 3. Updated OCRAM Memory Map

Start	End	Size	i.MX 6Dual/6Quad	i.MX 6DualPlus/6QuadPlus
0098_0000	009F_FFFF	512KB	OCRAM Aliased	OCRAM Aliased
0096_0000	0097_FFFF	128KB		OCRAM_3
0094_0000	0095_FFFF	128KB		OCRAM_2
0090_0000	0093_FFFF	256KB	OCRAM	OCRAM

The rest of the memory map will be the same as i.MX 6Dual/6Quad.

4.2 Interrupts

The i.MX 6DualPlus/6QuadPlus has four new PRE modules with one interrupt for each module.

Table 4. Updated Interrupt Table

IRQ	Interrupt Source
122	PRE0
129	PRE1
130	PRE2
131	PRE3

The other interrupt assignment will be the same as i.MX 6Dual/6Quad.

4.3 DMA

No changes as compared with i.MX 6Dual/6Quad.

5 Clock generation

The i.MX 6DualPlus/6QuadPlus Clock Control Module (CCM) will be based on i.MX 6Dual/6Quad.Changes required to support the improved GPU performance are as follows.

Table 5. Updated GPU2D Clock Root

Mux Input	i.MX 6Dual/6Quad		i.MX 6DualPlus/6QuadPlus	
	Frequency (MHz)	Source	Frequency (MHz)	Source
1	264	AXI	528	MMDC_CH0
2	480	PLL3 Main	480	PLL3 Main
3	352	PLL2 PFD0	594	PLL2 PFD1
4	396	PLL2 PFD2	720	PLL3_PFD0

Other changes are detailed as follows:

- New clock gating added to support the PRE and PRG modules. See the CCM CCGR6 register.
- The GPU 2D and 3D on the i.MX 6DualPlus/6QuadPlus are clocked differently and by default a faster 528 MHz AXI clock is provided.
- Oscillator clock option added to the UART, IPG, ECSPI and CAN clock roots. Additional clock options added to ENFC and CAN clock roots. The default settings are the same as i.MX 6Dual/6Quad. However to support the additional clock options, updates to the CCM CSCMRx, CSCDRx and CS2CDR registers were made.
- In i.MX 6Dual/6Quad there is a bug in the EMI clock root divider. See CSCMR1[22:20], bits 22 and 21. A read was inverted from the value written, resulting in the divider values not appearing to be sequential. This is corrected in i.MX 6DualPlus/6QuadPlus.
- The LDB_DIx_IPU clocks in i.MX 6Dual/6Quad are not clock gated. When changing the LDB clock source, glitches are possible, resulting in erratic behavior. Clock gating has been added to the LDB_DIx_IPU clocks in i.MX 6DualPlus/6QuadPlus to prevent glitch-related errors.
- In i.MX 6Dual/6Quad the MMDC Channel 1 clock gating control was not adjustable. In i.MX 6DualPlus/6QuadPlus, MMDC Channel 1 clock gating is now controllable. See the CCM CCDR register.
- CCM_CCR[7:0] default value changed to 0x7F from 0xFF in order to shorten 32 KHz XTAL lock time from 8 to 4 msecs.

6 Security

The i.MX 6DualPlus/6QuadPlus will have the same security architecture as i.MX 6Dual/6Quad.

The fuse map in i.MX 6DualPlus/6QuadPlus is updated to include a fuse bank for NXP use only and uses HAB version 4.1.1.

Table 6. Updated Fuse Map

Fuse Address	Description
0x0680 – 0x06CF	NXP use only, not to be modified by customers

This change to the fuse map means that i.MX 6DualPlus/6QuadPlus will not support DTCP key programming.

7 On-chip memories

The new Prefetch and Resolve feature added in i.MX 6DualPlus/6QuadPlus requires up to 256 KB OCRAM as a pixel pipeline buffer. In order to provide enough throughput, these 256 KB OCRAM are implemented as two 128 KB OCRAM instances, which will be known as OCRAM_2 and OCRAM_3.

OCRAM_2 and OCRAM_3 can be used as general purpose RAM when the Prefetch and Resolve features are not used. The OCRAM controllers for these new blocks and the existing OCRAM controllers will be updated to support simultaneous read/write access, improving access efficiency.

The other on-chip memories remain the same as i.MX 6Dual/6Quad.

8 External memory

The i.MX 6DualPlus/6QuadPlus will have the same external Memory as i.MX 6Dual/6Quad.

Although the DRAM controller and frequency will remain the same, the overall DRAM utilization is significantly improved, due to the improvements in the bus fabric and graphics IP.

The DRAM controller has also been enhanced with additional trim controls for the SDCLKx and SDQSx signals.

This updated fine tuning control has been copied from the i. MX 6SoloX family of processors, where it has been successfully verified on actual products.

These new trim controls allow additional fine tuning to enable i.MX 6DualPlus/6QuadPlus to adhere to the JEDEC timing specification.

Each of the following signals has independent trim control, via the register and bit field shown in the following table.

Table 7. Additional DRAM trim controls

Signal Name	Control Field	Bit Name
SDCLK		
DRAM_SDCLK_0	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR00[9:8]	SDCLK_0_TRIM
DRAM_SDCLK_0_B	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR00[17:16]	SDCLK_0_B_TRIM
DRAM_SDCLK_1	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR01[9:8]	SDCLK_1_TRIM
DRAM_SDCLK_1_B	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR01[17:16]	SDCLK_1_B_TRIM
DQS		
DRAM_SDQS0	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR02[9:8]	SDQS0_TRIM
DRAM_SDQS0_B	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR02[17:16]	SDQS0_B_TRIM
DRAM_SDQS1	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR03[9:8]	SDQS1_TRIM
DRAM_SDQS1_B	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR03[17:16]	SDQS1_B_TRIM
DRAM_SDQS2	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR04[9:8]	SDQS2_TRIM
DRAM_SDQS2_B	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR04[17:16]	SDQS2_B_TRIM
DRAM_SDQS3	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR05[9:8]	SDQS3_TRIM
DRAM_SDQS3_B	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR05[17:16]	SDQS3_B_TRIM
DRAM_SDQS4	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR06[9:8]	SDQS4_TRIM
DRAM_SDQS4_B	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR06[17:16]	SDQS4_B_TRIM
DRAM_SDQS5	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR07[9:8]	SDQS5_TRIM
DRAM_SDQS5_B	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR07[17:16]	SDQS5_B_TRIM
DRAM_SDQS6	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR08[9:8]	SDQS6_TRIM

Table 7. Additional DRAM trim controls (continued)

DRAM_SDQS6_B	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR08[17:16]	SDQS6_B_TRIM
DRAM_SDQS7	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR09[9:8]	SDQS7_TRIM
DRAM_SDQS7_B	IOMUX_SW_PAD_CTL_PAD_DRAM_ADDR09[17:16]	SDQS7_B_TRIM

The 2-bit control field for each signal is defined as shown in the following table.

Table 8. SDCLK_x_TRIM and SDQS_x_TRIM control definitions

BitField	Description
00	No additional delay
01	1 delay unit added to pad edge
10	2 delay units added to pad edge
11	3 delay units added to pad edge

A single delay unit is typically defined as 30 ps.

Further trimming controls have also been added to the hardware ZQ calibration process. This allows an offset to be applied to the ZQ_HW_PU_RES and ZQ_HW_PD_RES fields in the MMDC_MPZQHWCTRL[15:6] register.

The offset range is programmable from -7 to +7, controlled by the ZQ_PU_OFFSET and ZQ_PD_OFFSET fields in the MMDC_MPPDCMPR2[11:4] register. Enabled by the ZQ_OFFSET_EN bit, also in the MMDC_MPPDCMPR2[3] register.

Updates to the bus interface make it possible to perform some of the arbitration and reordering functions outside of the MMDC block, offering improved performance. To support this the following controls have been added to disable functions within the MMDC block.

Table 9. Arbitration and reordering controls

Bit Name	Description
MMDC_MAARCR[26]	Disable all MMDC arbitration and reordering controls
MMDC_MAARCR[25]	Disable MMDC reordering controls only

To avoid potential conflict, the corresponding bus controls must match these new MMDC settings. The bus controls are defined by the BOOT_CFG3[5:4] and BOOT_CFG3[1:0] bits.

Table 10. BOOT_CFG3[5:4] bus settings

BOOT_CFG3[5:4]	Description
00	Single DDR channel mapping, NOC scheduler enabled, MMDC reorder disabled
01	Fixed 2x32 mapping, NOC scheduler disabled, MMDC reorder enabled
10	4KB interleaving mapping, NOC scheduler disabled, MMDC reorder enabled
11	Extension mode (See BOOT_CFG3[1:0] settings)

Table 11. BOOT_CFG3[1:0] bus settings, only valid when BOOT_CFG3[5:4] = 0b11

BOOT_CFG3[1:0]	Description
00	Single DDR channel mapping, NOC scheduler disabled, MMDC reorder enabled
01	Fixed 2x32 mapping, NOC scheduler enabled, MMDC reorder disabled
10	Reserved
11	Reserved

9 Display

In i.MX 6DualPlus/6QuadPlus, a new function named IPU Prefetch and Resolve is introduced on top of the current IPU-based display subsystem. The concept of Prefetch and Resolve is comprised of two primary functions:

- Prefetch: Use Prefetch and Resolve Engine (PRE) to read the display frame buffer ahead of time and store it into double buffer in OCRAM. When IPU needs the pixels for display, it can fetch directly from the double buffer. This helps to avoid a potential IPU display under-run in high loading applications, making the system more robust.
- Resolve: When the frame buffer is a GC2000 GPU render target buffer (unresolved tiled buffer format from GC2000), the PRE will resolve it from a tiled to linear buffer format and store into OCRAM, so that the IPU can display the resolved buffer directly. This helps to avoid an additional resolve operation in the GC2000, saving DRAM bandwidth.

The basic data flow is shown in the following diagram.

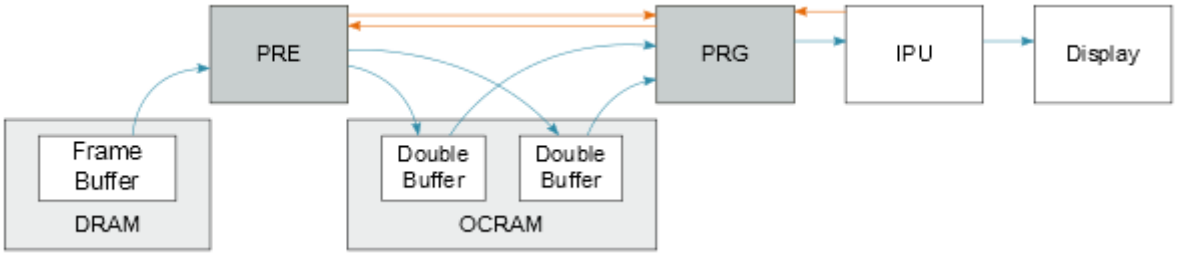

Figure 2: Prefetch and Resolve Data Flow

There is a Prefetch and Resolve Gasket (PRG) block in front of the IPU. The purpose of this block is to perform a handshake between PRE and IPU for flow control. The double buffer inside OCRAM is only 4/8/16 lines, once the PRE fills one buffer, it will generate a ready signal to the PRG, and the PRG will subsequently allow the IPU to read this buffer. After the IPU has finished reading one buffer, the PRG will generate a done signal to the PRE module so it can recycle this buffer and start prefetching pixels into it.

The input buffer format supported/not supported by PRE is summarized in the following table.

Table 12. Input Buffer Format

Type	Buffer Format	Supported by PRE
Unresolved Tile Buffer	Standard 4x4 Tile Buffer	Supported
	Super Tile	Supported
	Split Super Tile	Supported
	Split GPU Tiled Buffer	Supported
	Fast Clear Tile Buffer	Not supported
Resolved Linear Buffer	Compressed Tile Buffer	Not supported
	2x MSAA Tile Buffer	Not supported
	Generic Date (1-plane)	Supported
	RGB/ARGB (1-plane)	Supported
	YUV (1-plane/2-plane/3-plane)	Supported

Each buffer required for prefetch is at least 4 lines. The double buffer size for one prefetch resolve operation is calculated as: HSIZE x BPP x 4 lines x 2. The following table shows the memory requirement for some typical use cases.

Table 13. OCRAM Requirement for Prefetch and Resolve

Use Case	PRE-0	PRE-1	PRE-2	PRE-3	Total
1x 1920x1080@60fps	60KB	—	—	—	60KB
2x 1920x1080@60fps	60KB	60KB	—	—	120KB
2x 1920x720@75fps	60KB	60KB	—	—	120KB
4x 1280x720@60fps	40KB	40KB	40KB	40KB	160KB
4x 1920x1080@60fps	60KB	60KB	60KB	60KB	240KB

For the 4x PRE blocks, PRE-0 is dedicated to IPU-1, PRE-3 is dedicated to IPU-2, PRE-1 and PRE-2 can be configured to be used together with either IPU-1 or IPU-2. The following table shows the valid assignments:

Table 14. PRE to IPU assignment

Port	PRE-0	PRE-1	PRE-2	PRE-3
Mode 1	IPU-1	IPU-1	IPU-2	IPU-2
Mode 2	IPU-1	IPU-1	IPU-1	IPU-2
Mode 3	IPU-1	IPU-2	IPU-2	IPU-2

The PRE module is attached to IPU DMA virtual channels. Each IPU can have up to 3 PRE assigned to its 3 DMA channels. There is no hardware restriction on how the PRE is used for physical displays. For example, two PRE can be assigned to two DMA channels which drives two individual displays, or the two PRE modules can be assigned to two DMA channels which are combined in the IPU DP sub block and drives only one display. The diagrams below show some typical use cases for PRE in conjunction with the IPU.

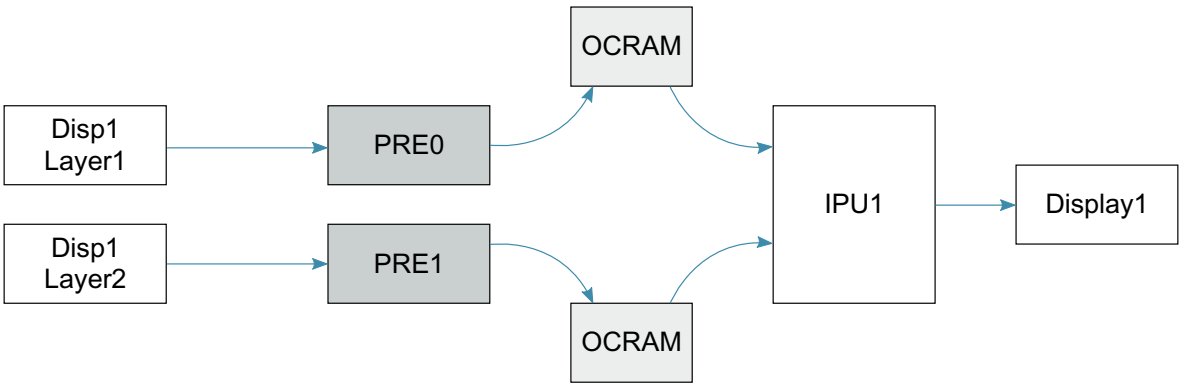

Figure 2. Single Display with Two PRE

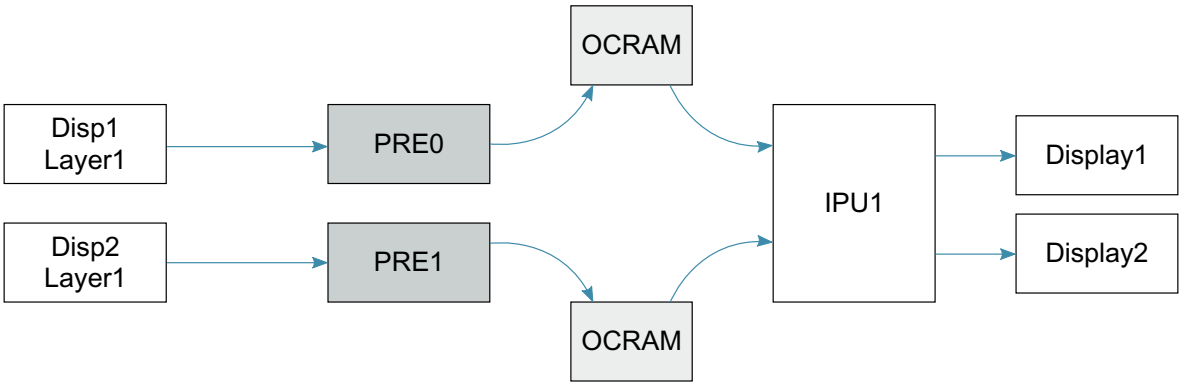

Figure 3. Dual Display with Two PRE

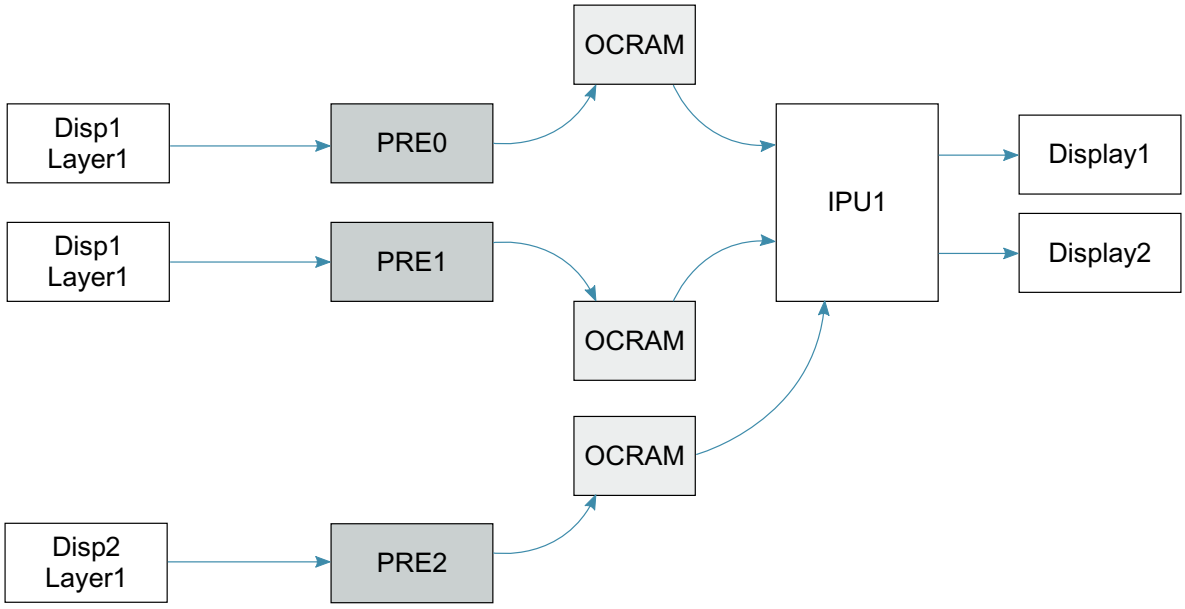

Figure 4. Dual Display with Three PRE

10 Prefetch and Resolve restrictions

Two functions on the IPU cannot be used when Prefetch and Resolve function is enabled:

- Automatic Scrolling. IPU supports moving image (scrolling) automatically by reading frames (from a background buffer) with incremental offset. This function cannot be supported with PRE.
- Conditional Read. IPU supports a conditional read access to external memory based on the alpha value. This is achieved by reading an alpha buffer first and blocking access to frame buffer based on alpha value. This function cannot be supported with PRE.

The other display functions will remain the same as in i.MX 6Dual/6Quad.

11 Graphics

The most important change on i.MX 6DualPlus/6QuadPlus is the graphics performance improvement. In addition to the optimization on bus fabric, the graphics engines themselves are also updated for performance, including:

- Optimize the data flow between the graphics display engine to reduce memory accesses.
- Optimize the data access from the graphics engine to improve DRAM efficiency.
- Increase target frequency of the graphics engines.
- Fixed errata:
  - ERR004300 - GPU3D: L1 cache performance drop
  - ERR004484 - GPU3D: L1 cache "Write Address Data" pairing error
  - ERR005216 - GPU3D: Black texels in Android App Singularity 3D
  - ERR005908 - GPU2D: Image quality degradation observed for stretch bits when the stretch factor is exactly an integer

11.1 Buffer format support

The GC2000 GPU uses its own tiled buffer format when it renders a target. In i.MX 6Dual/6Quad, some of the render targets (tiled buffers) cannot be used by the graphics engines as the source buffer, including the GC2000 itself. It has to be resolved by GC2000 into linear buffer first. This resolve operation causes extra traffic to the DRAM and reduces the overall graphics performance. In i.MX 6DualPlus/6QuadPlus, the GC320 is updated to support reading the GC2000 render targets to avoid resolve operations.

The following table summarizes the different buffer format support between i.MX 6Dual/6Quad and i.MX 6DualPlus/6QuadPlus.

Table 15. Buffer Format Support for GPU

Number of Buffers	Buffer Format	GC2000		GC320		GC355	
		INPUT	OUTPUT	INPUT	OUTPUT	INPUT	OUTPUT
1	Linear	Y	Y-DQP N-DQ	Y	Y	Y	Y
1	Tile	Y	Y-DQP N-DQ	Y	N	Y	N
1	Super Tile	Y	Y-DQP N-DQ	Y	N	N	N
2	Split Tile	N	Y	Y-DQP N-DQ	N	N	N
2	Split Super Tile	N	Y	Y-DQP N-DQ	N	N	N

The GC2000 also supports a compressed buffer format to reduce DRAM accesses. In i.MX 6Dual/6Quad, when the GC2000 reads a compressed tile, its burst size is reduced from 64-bytes to 32/16-bytes. However, in a system with a 64-bit DDR3, each DRAM access is fixed to 64-bytes. Although the data read by the GC2000 is reduced, the access to DRAM remains the same. In i.MX 6DualPlus/6QuadPlus, the GC2000 will optimize read operations for bandwidth saving.

11.2 Multiple overlay support

In several customer use case applications, there will be multiple overlays on the final display. The GC320 in i.MX 6Dual/6Quad only supports composition on two layers, so there will be multiple composition operations required to support multiple overlays if the GC320 is used as the composition engine. This causes a lot of extra read/write accesses to the DRAM. In order to reduce the traffic, the GC320 will be updated to support composition on 8 layers.

11.3 GPU enhancements

Table 16. Graphics Engine Target Frequency

Name	Clock	i.MX 6Dual/6Quad	i.MX 6DualPlus/6QuadPlus
GC2000	AXI/Core/Shader	264MHz / 528MHz / 594MHz	528MHz / 594MHz / 720MHz
GC320	AXI/Clk2x	264MHz / 480MHz	528MHz / 720MHz
GC355	AXI/Clk2x	264MHz / 480MHz	528MHz / 720MHz

The GC2000 also features an increased cache size, shader register count and vertex/texture inputs for improved vertex and fragment shader performance.

Table 17. Enhanced GC2000 Features

Description	i.MX 6Dual/6Quad	i.MX 6DualPlus/6QuadPlus
Index Buffer	512 Bytes	1 KBytes
Vertex Cache	1 KBytes	2 KBytes
Vertex DMA Streams	8	16
Uniform Registers (128-bit)	Vertex shader: 168; Fragment shader: 64	320 unified
Max Shader Instructions	512 unified	1 M (with I-cache) per shader type
Texture Sampler Units	12	32
Max Textures Per Fragment	8	16
Texture Cache	2 KByte	12 KByte
Multiple Render Targets	8	16

12 Video

The i.MX 6DualPlus/6QuadPlus will have the same video subsystem as i.MX 6Dual/6Quad. However, increased performance can be observed in some specific VPU use cases that were previously DDR Bandwidth limited.

Refer to the GPU performance comparison demo, available at:
http://www.nxp.com/video/i.mx-6dualplus-and-i.mx-6quadplus:IMX6-DUALPLUS-QUADPLUS

13 Peripherals

The i.MX 6DualPlus/6QuadPlus will have the following changes on peripherals:

- Added a mux to the ENET reference clock to enable clocking direct from ENET PLL. In i.MX 6Dual/6Quad, the reference clock must be sourced from ENET_TX_CLK pad.
- To provide better external chip support, the ENET_1588_EVENT0_OUT signal has a programmable pulse width. Using IOMUXC_GPR0[9:8] pulse width can be programmed from 1 to 4 clock pulses. The other three ENET_1588_EVENTx_OUT signals are as before on i.MX 6Dual/6Quad. It should be noted however, if ENET_1588_EVENT0_OUT is programmed for 1 clock pulse width it will appear 1 clock pulse delayed relative to the other ENET_1588_EVENTx_OUT signals, which is different from i.MX 6Dual/6Quad.
- There is a BCH bug in i.MX 6Dual/6Quad that is not currently listed in the errata, but it is fixed in i.MX 6DualPlus/6QuadPlus.
  - When BCH_MODE[ERASE_THRESHOLD] is non-zero BCH_STATUS0[ALLONES] is set, even if there are bit flips (zeros) in the payload buffer. In i.MX 6DualPlus/6QuadPlus a new register was added, BCH_DEBUG1[9:0], which provides a count of the zero bits in an erased page.
- Fixed errata:
  - ERR005723 - PCIe: PCIe does not support L2 power down.

— ERR006687 - ENET: Only the ENET wake-up interrupt request can wake the system from Wait mode.
— ERR007966 - SATA: SATA speed negotiation fails after suspend and resume.

The other peripheral functions in i.MX 6DualPlus/6QuadPlus will be same as i.MX 6Dual/6Quad.

14 Analog

The i.MX 6DualPlus/6QuadPlus will have the following analog changes:

- The default output on ARM, SOC and PU LDOs will be changed to 1.15V (1.1V on i.MX 6Dual/6Quad).
- After an SNVS power on reset event the processor will use the internal ring oscillator to provide the CKIL clock for 16,000 clock cycles, before switching to the external 32KHz source, if present, otherwise it will continue to use the internal clock. This provides an approximate 0.5 second stabilization delay at power on, assuming the internal ring oscillator is running at 32KHz.
- The internal ring oscillator tolerance has been improved, matching the performance of the other members in the i. MX processor family. The ring oscillator will operate within the range of 24 to 44 KHz, in i.MX 6Dual/6Quad opertaion up to 66 KHz was possible.
- Added logic to automatically reset PFDs to prevent clock glitches on power up or when associated PLL state is changed from disabled to enabled.
- Revision ID register value changed to 0x630100.

The other Analog functions in i.MX 6DualPlus/6QuadPlus will remain the same as i.MX 6Dual/6Quad.

15 I/O design

The IO pad in i.MX 6DualPlus/6QuadPlus will be the same as in i.MX 6Dual/6Quad.

16 PINMUX

The i.MX 6DualPlus/6QuadPlus will be the same PINMUX as in i.MX 6Dual/6Quad with one exception. i.MX 6Dual/6Quad documentation incorrectly shows SDMA_EXT_EVENT0 muxed to the DISP0_DATA16 pad. This is not supported in i.MX 6Dual/6Quad, only SDMA_EXT_EVENT1muxed to the DISP0_DATA17 pad is supported in i.MX 6Dual/6Quad. This has been corrected in i.MX 6DualPlus/6QuadPlus and both SDMA_EXT_EVENT0 and 1 are supported.

Table 16-18. SDMA External Event Support

i.MX	SDMA Ext Event0 / Channel	SDMA Ext Event1 / Channel
6DLS	DISP0_DATA16 or GPIO17 / Channel 2	DISP0_DATA17 or GPIO18 / Channel 14
6DQ	-	DISP0_DATA17 or GPIO18 / Channel 14
6DQP	DISP0_DATA16 or GPIO17 / Channel 47	DISP0_DATA17 or GPIO18 / Channel 14

17 Package

The i.MX 6DualPlus/6QuadPlus will be the same package and ball map as in i.MX 6Dual/6Quad.

18 Power

The power architecture of i.MX 6DualPlus/6QuadPlus will be the same as i.MX 6Dual/6Quad.VDD_HIGH and VDD_SNVS are specified to a maximum 3.3 volts on i.MX 6Dual/6Quad, this will be changed to 3.6 volts on i.MX 6DualPlus/6QuadPlus. Because of the change in GPU, bus fabric and other modules in the VDD_SOC domain, the max power consumption on VDD_SOC will increase compared to i.MX 6Dual/6Quad.Similarly, since the DRAM efficiency will be improved, the power consumption on NVCC_DRAM is also expected to be higher than i.MX 6Dual/6Quad. All other power rails should remain the same as i.MX 6Dual/6Quad.

Refer to the latest relevant data sheet (IMX6DQPAEC - Automotive, IMX6DQPCEC - Consumer, IMX6DQPIEC - Industrial) for the appropriate power consumption figures.

NXP recommends using the PF0100 PMIC that has specific OTP options (F9 and FA) that mate with the i.MX 6DualPlus/6QuadPlus. These OTP options are backward compatible with the i.MX 6Dual and i.MX 6Quad. This provides a single power solution for i.MX 6Dual/6Quad and i.MX 6DualPlus/6QuadPlus while also providing sufficient margin for the worst case load currents.

19 System boot

The overall system boot flow in i.MX 6DualPlus/6QuadPlus will remain the same as i.MX 6Dual/6Quad, including the boot device type and configuration.

The ROM code has been updated to reflect and support the increased OCRAM free space, with the inclusion of OCRAM_2 and OCRAM_3, supporting larger firmware images, which required the ROM code MMU table, stack and vectors to be relocated at the end of the 512 KB block.

The valid range of registers in the DCD field has been updated to include the new bus fabric blocks, required to support changes in DDR initialization, that will enable the improved DDR performance.

In i.MX 6Dual/6Quad there is a potential issue for customers who are booting from, and mass programming NAND devices off-board. If all devices are programmed with the same FCB, including the same starting page, that will result in boot failure in the rare occasions that the starting page is marked as a bad block. In i.MX 6DualPlus/6QuadPlus the ROM code will skip to the next good block if the starting page is marked as a bad block.

In i.MX 6Dual/6Quad after the ROM code uses the HAB API to authenticate the u-boot image, it sets a flag in memory to indicate the cache is disabled. When u-boot attempts to use the same HAB API for the kernel image, the cache appears disabled, resulting in a slower authentication. This requires a workaround in u-boot. In i.MX 6DualPlus/6QuadPlus the HAB API verifies the cache status in a hardware register, not a flag in memory.

The revision value will be updated to 2.0.

In addition the following errata are fixed:

- ERR005768 - ROM: In rare cases, secondary image boot flow may not work due to mis-sampling of the WDOG reset
- ERR007926 - ROM: 32 kHz internal oscillator timing inaccuracy may affect SD/MMC, NAND, and OneNAND boot

20 Temperature

Due to increased power consumption, thermal management techniques may be required to keep the i.MX 6DualPlus/6QuadPlus below the specified junction temperature.

Refer to the appropriate data sheet (AEC, CEC, or IEC) to determine the supported junction temperature.

21 References

i.MX 6Dual/6Quad Applications Processor Reference Manual (IMX6DQRM)

i.MX 6Dual/6Quad and 6DualPlus/6QuadPlus Chip Errata (IMX6DQCE)

i.MX 6Dual/6Quad Applications Processors for Automotive Products - Datasheet (IMX6DQAEC)

i.MX 6DualPlus/6QuadPlus Applications Processor Reference Manual (IMX6DQPRM)

i.MX 6DualPlus/6QuadPlus Applications Processors for Automotive Products - Datasheet (IMX6DQPAEC)

i.MX 6DualPlus/6QuadPlus Applications Processors for Consumer Products - Datasheet (IMX6DQPCEC)

i.MX 6DualPlus/6QuadPlus Applications Processors for Industrial Products - Datasheet (IMX6DQPIEC)

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