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SDCLK Duty Cycle Optimizations for i.MX 6Quad/6Dual

1. Introduction

The default software configuration of the MMDC SDCLK clock duty cycle registers on the i.MX 6Quad/6Dual SoCs are not optimal to comply with the clock duty cycle parameter as specified in the JEDEC DDR3 SDRAM Standard JESD79-3.

This document briefly describes the NXP recommended software changes to better align the duty cycle of the DRAM_SDCLK0 and DRAM_SDCLK1 on the i.MX 6Quad/6Dual SoCs with JEDEC standards. No data integrity issues have been observed due to this non – optimal setting. There are no hardware changes being proposed to better align the SDCLK clock duty cycle to the JEDEC specification, only certain register changes are being proposed in the software initialization of the DDR.

The document also briefly describes additional methods to further optimize the duty cycle however these are not absolutely necessary and may have limited applicability on certain customer board designs.

Contents

2. MMDC SDCLK Duty Cycle Control Fine Tuning

The i.MX 6Dual/6Quad Multi Mode DDR Controller (MMDC) has the ability to fine tune the duty cycle of the DRAM_SDCLK0 and DRAM_SDCLK1 clock signals as well as the DQS clock signals.

This is accomplished by modifying the MMDC Duty Cycle Control Register 1 (MMDC1_MPDDCR) for DRAM_SDCLK0 and MMDC Duty Cycle Control Register 2 (MMDC2_MPDDCR) for DRAM_SDCLK1 respectively. MMDC1_MPDCCR register is mapped to AXI channel 0 and MMDC2_MPDCCR is mapped to AXI channel 1.

Programming of these registers after initialization is only permitted by entering the DDR device into self-refresh mode through LPMD/DVFS mechanism. Therefore, it is recommended to modify these registers in the initial MMDC configuration performed by the software boot loader.

The following bits in the MMDC Duty Cycle Control Registers are used to control the duty cycle of the clock (DRAM_SDCLK0/1).

- **CK_FT0_DCC** : Primary duty cycle fine tuning control of the DDR clock
- **CK_FT1_DCC** : Secondary duty cycle fine tuning control of the DDR clock

Settings of these register bits are as follows:

Table 1. MMDC Duty Cycle Control Registers - CK_FTx_DCC Bit Settings

CK_FTx_DCC Bit Setting	Duty Cycle Impact	Notes
001b	Reduce by 3.0 %	Actual duty cycle reduction may vary
010b	No Change	Out of reset default register setting
All other settings	Reserved	Software should not program any other settings in the CK_FTx_DCC bit field

The adjustments are cascaded which means that adjustment FT0 is applied first, and then adjustment FT1 is applied to the result of the first adjustment. If an adjustment of 3.0 % is desired, either stage CK_FT0_DCC or stage CK_FT1_DCC can be used. If a larger adjustment is desired, then both stages CK_FT0_DCC and CK_FT1_DCC are used, and applied in the same direction.

2.1. JEDEC Specification

The JEDEC DDR3 SDRAM Standard JESD79-3 specifies the following clock timing parameters:

Table 2. JEDEC clock timing parameters

Parameter	Symbol	Min	Max	Units
Average High Pulse Width	tCH(avg)	0.47	0.53	tCK(avg)
Average Low Pulse Width	tCL(avg)	0.47	0.53	tCK(avg)

The DDR3 SDCLK0 and SDCLK1 pulse width or duty cycle should be between 47 and 53 % of the average clock period - tCK(avg).

3. Recommended SDCLK Duty Cycle Fine Tune Settings

Design simulations combined with actual circuit measurements over worse case silicon process and temperature conditions have yielded the following settings to be the optimal for Duty Cycle performance which gives the best margin on memory stress testing with Auto ZQ calibration enabled.

Table 3. Recommended Duty Cycle Fine Tune parameter settings

Clock	Register	CK_FT0_DCC	CK_FT1_DCC	Notes
SDCLK0	MMDC1_MPDDCR Address: 0x021B_08C0	010b	001b	Since CK_FT0_DCC = 0x2 is the default value out of reset, the only change required is modifying the CK_FT1_DCC to 0x1
SDCLK1	MMDC2_MPDCCR Address 0x021B_48C0	010b	001b	Since CK_FT0_DCC = 0x2 is the default value out of reset, the only change required is modifying the CK_FT1_DCC to 0x1

NOTE

The above recommended configuration of SDCLK1 in MMDC2_MPDCCR is not required for applications not using SDCLK1

NOTE

The following recommendations are based on measurements on NXP hardware and are presented as guidelines for the customer. Variations due to the different board layouts, topology, memory selection, components and other various factors can yield slightly different results. Customers are recommended to optimize parameters for their end product appropriately.

Default Values of MMDC1_MPDDCR and MMDC2_MPDDCR registers after reset

```
0x021b08c0 = 0x24922492   // MMDC1_MPDDCR
0x021b48c0 = 0x24922492   // MMDC2_MPDDCR
```

Proposed Register Configuration for MMDC1_MPDDCR and MMDC2_MPDDCR

```
0x021b08c0 = 0x24921492   // Recommended MMDC1_MPDDCR setting
0x021b48c0 = 0x24921492   // Recommended MMDC2_MPDDCR setting
```

The recommended location for inserting the MMDC_MPDDCR registers settings for modifying the SDCLK duty cycle adjustments during the MMDC initialization would be immediately after the Program Calibration Setting Registers and before issuing the MMDCx_MPMUR0_FRC_MSR command to set calibration values in the PHY. An example is shown below:

Example 1. Duty cycle adjustment in DDR initialization scripts

```
//Duty Cycle Adjustment in DDR Initialization scripts

//==================================================================

// Write Leveling calibration

// Read DQS Gating calibration

// Read calibration

// Write calibration

// Duty Cycle adjustment

setmem /32       0x021b08c0 =     0x24921492
setmem /32       0x021b48c0 =     0x24921492

//==================================================================

// Complete calibration by forced measurement:

//MMDC init:
```

SDCLK Duty cycle optimizations for i.MX 6DualPlus/6QuadPlus are discussed in *MMDC & NoC Configuration for Optimal DDR3 Performance on the i.MX 6DualPlus/6QuadPlus* (document *EB828*)

4. Other Recommendations to Improve SDCLK Duty Cycle

The following section provides recommendations on how to further optimize the duty cycle however that are not absolutely necessary to bring the Duty Cycle into the JEDEC specification. These recommendations may also have limited applicability on certain customer designs.

4.1. Drive Strength Configuration

Testing has shown that lowering the drive strengths from the maximum value in the IOPAD Drive Strength Field (DSE= 111b) will improve the SDCLK Duty Cycle even further, but is not absolutely necessary to bring the Duty Cycle into the JEDEC specification. For the IOPAD Drive Strength users can set the DSE = 110b (40 Ohms (default value) bits 5, 4, 3) in the IOMUXC_SW_PAD_CTL_PAD_DRAM_XX registers.

Please note that drive strength configuration and optimization is dependent on the customer board layout and design. Depending on the design it may not be possible to lower drive strengths.

4.2. VDD_SOC_CAP Configuration

NXP testing has shown that lowering the VDD_SOC_CAP voltage level from the specification maximum will improve the SDCLK Duty Cycle marginally, but is not absolutely necessary to bring the Duty Cycle into the JEDEC specification.

The VDD_SOC_CAP voltage level setting can be reduced in the PMU_REG_CORE register in the Power Management Unit (PMU). Please note that the VDD_SOC_CAP optimization is dependent on the customer design and the operating ranges defined in the respective i.MX 6Dual/6Quad - segment Data Sheets. Depending on the customer design and restrictions it may not be possible to lower the VDD_SOC_CAP voltage level.

4.3. Clock Jitter Reduction

Regulation instabilities and ripples on the output of the LDO can also increase the system clock jitter which can impact the Duty Cycle. Specifically ensure correct capacitors sizing and placement on NVCC_PLL_OUT , VDD_SOC_CAP and VDD_HIGH_CAP.

To minimize jitter follow the layout and decoupling recommendations in the *i.MX6 Hardware Development Guide for i.MX 6Quad, 6Dual, Families of Applications Processors* (document IMX6DQ6SDLHDG).

5. References

1. JEDEC DDR3 SDRAM Standard JESD79-3 F (document JESD79-3 F)
2. *i.MX6 Hardware Development Guide for i.MX 6Quad, 6Dual, Families of Applications Processors* (document IMX6DQ6SDLHDG)
3. *i.MX 6Dual/6Quad - Segment Data Sheets* (documents IMX6DQCEC, IMX6DQAEC, and IMX6DQIEC)
4. *i.MX 6Dual/6Quad Applications Processor Reference Manual* (document IMX6DQRM)
5. *MMDC & NoC Configuration for Optimal DDR3 Performance on the i.MX 6DualPlus/6QuadPlus* (document EB828)

6. Revision History

Table 4. Revision History

Revision number	Date	Substantive changes
0	08/2016	Initial release

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